July 2015

CURRICULUM VITAE

Name: PANAGIOTA

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Date of birth: JUNE 01, 1970

Place of birth: DRAMA, GREECE

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CURRENT OCCUPATION

2003- June 2012, Application Professor, Department of Science, Technological Education Institute of Kavala.

June 2012 – Septembre 2013, Assistant Professor, Department of Science, Technological Education Institute of Kavala.

Septembre 2013– to pressent, Assistant Professor, Department of Electrical Engineering, Eastern Macedonia and Thrace Institute of Technology.

COURSES

1. Physics Laboratory.
2. Electromagnetic Theory.
3. Microprocessor – Microcomputers (Lectures and Laboratory)
4. Electronics I (Lectures and Laboratory)
5. Electronics II (Lectures)
6. Electrical Circuits I (Lectures)
7. Electrical Circuits I I(Lectures)
8. Digital Electronics (Laboratory)

EDUCATION - DEGREES

1. **1993, BSc** in Physics from the Aristotle University of Thessaloniki, Greece.
2. **1996, MSc** in Electronic Physics (Radioelectrology) from the Aristotle University of Thessaloniki Department of Physics, Greece.

3. **2002, Ph.D.** degree in Microelectronic from Democritus University of Thrace, Department of Electrical Engineering, Xanthi, Greece.

SCIENTIFIC EXPERIENCE

FIELDS OF SCIENTIFIC ACTIVITY:

- Semiconductor Device Modeling, Simulation and Fabrication.

RESEARCH AREAS OF INTEREST:

- Microelectronic Devices and Applications.
- Photodiodes and Optoelectronic Semiconductor Devices.
- Semiconductor Device Modeling, Simulation and Fabrication.
- Electrical and Optical Semiconductor Device Characterization.

THESIS - LIST OF PUBLICATIONS

1. THESIS

1.1. **2002, «Design, Fabrication, Characterization and Simulation of silicon p^{+}np Bulk - Barrier diodes»,** Ph. D. thesis, Laboratory of Electrical and Electronic Materials Technology, Department of Electrical and Computer Engineering, Democritus University of Thrace, Xanthi, Greece.

2. REACHERS PAPERS

2.1. **P. Papadopoulou, N. Georgoulas, L. Georgopoulos, A. Thanailakis, «A model for the dc electrical behavior of Bulk-Barrier Diodes»,** Electrical Engineer, Archiv fur Elektrotechnik, Vol. 83 (4), pp. 203-211 (2001).

2.2. **P. Papadopoulou, N. Georgoulas and A. Thanailakis, «Simulation and Experimental Results on the Switching Behaviour of Bulk-Barrier Diodes»,** Microelectronics Journal, Vol. 33 (5-6), pp. 487-494 (2002).

2.3. **P. Papadopoulou, N. Georgoulas and A. Thanailakis, «An extensive study of the photocurrent amplification mechanism of silicon Bulk - Barrier**

diodes based on simulation and experimental results», Thin Solid Film, Vol. 415, pp. 276-284 (2002).

2.4. **P. Papadopoulou, N. Georgoulas , L. Magafas, «A study of the optical response speed of silicon Bulk -Barrier photodiodes based on simulation results»,** Optoelectronics and Advanced materials - Rapid Communications Vol. 1, No. 8, p. 379 - 384 (2007).

2.5. **P. Papadopoulou, Ant. Meletis, G. Doukakis, C. Mertzanidis, «Frequency Domain Response of Dielectrics for TE Plane Waves»,** European Journal of Scientific Research, Vol. 34, No.4, pp.463-473 (2009).

2.6. **P. Papadopoulou, L. Georgopoulos «A study of the silicon Bulk-Barrier Diodes designed in planar technology by means of simulation»** Journal of Engineering Science and Technology Review, Vol. 2, pp. 157-164, (2009).

2.7. **M.Hanias, L.Magafas, S.Stavrinides, P.Papadopoulou and M.Ozer, «Chaotic behavior of the forward I-V characteristic of the Al/a-SiC:H/c-Si(n) heterojunction Complexity»,** Proceedings of the 4th International Interdisciplinary Chaos Symposium, p.221,(2013), Chaos and Complex Systems 2013, pp 475-479.

2.8. **P. Papadopoulou, S. Stavrinides, M. Hanias, L. Magafas, «Study of the Electrical Behavior of Metal/_-SiC:H/poly-Si(N) Structure Using Simulation»,** Proceedings of the 4th International Congress APMAS2014, Acta Physica Polonica, Vol. 127 no 4 (2015).

3. CONFERENCES

3.1. **P. Papadopoulou, L. Georgopoulos, N. Georgoulas, A. Thanailakis, «Stimulation of Electrical and Optical behaviour of Bulk-Barrier diodes»,** XIII Greek Solid State Physics Conference, Thessaloniki 22-24 September 1997.

3.2. **P. Papadopoulou, N. Georgoulas, A. Thanailakis, «Transient analysis of Bulk-Barrier diodes using simulation»**, XIV Greek Solid State Physics Conference, Ioannina 15-18 September 1998.

3.3. **P. Papadopoulou, N. Georgoulas, A. Thanailakis, «Study of the switching behaviour of silicon Bulk-Barrier photodiodes in light pulse using simulation»,** XV Greek Solid State Physics Conference, Patra 27-29 September 1999.

3.4. **P. Papadopoulou, N. Georgoulas, A. Thanailakis, «Influence of the light modulation frequency on the external quantum efficiency of silicon p^{+}np photodiodes»,** XVII Greek Solid State Physics Conference, Xanthi 6-9 September 2001.

3.5. **P. Papadopoulou, L. Georgopoulos, N. Georgoulas, «Study of the influence of the incident light power on the optoelectronic behaviour of silicon p^{+}np photodiodes»,** XXI Greek Solid State Physics Conference, Nicosia Cyprus, 28-31 August 2005.

REFERENCES

2.1

1. **P. Papadopoulou, et al.,** Microelectronics Journal, Vol. 33 (5-6), pp. 487-494 (2002).
2. **P. Papadopoulou, et al.,** Thin Solid Film, Vol. 415, pp. 276-284 (2002).
3. **C. M. Sun et al.,** Nuclear Instruments & Methods in Physics Research A, Vol. 547, pp. 437 - 449 (2005).

2.2

1. **Der-Feng Guo,** IEEE Electron Device Letters, Vol. 24, No3, pp. 162 - 164, (2003).
2. **Der-Feng Guo, et al.,** IEEE Transactions on Electron Devices, Vol.51, No. 4, pp. 542 - 547, (2004).
3. **Jing-Yuh Chen,** «Investigation of InP- based Heterojunction Bipolar Transistors and Optoelectronic Switching Devices», Ph.D. Thesis Institute of

Microelectronics, Department of Electrical Engineering, National Cheng Kung University Tainan, Taiwan (2005).

4. **Der-Feng Guo,** Optoelectronics, IEE Proceedings, Vol.153, No.2, pp.63 -66, (2006).
5. **Weng, T.-Y., et al.,** Conference on Optoelectronic and Microelectronic Materials and Devices, Proceedings, COMMAD, Article No. 4429888, pp. 94-97, (2006).
6. **Der-Feng Guo,** Journal of the Electrochemical Society, Vol.154, No.1, pp. H13 - H15, (2007).
7. **Der-Feng Guo, et al.,** Surface Review and Letters, Vol.15, Issue 1-2, pp 139-144, (2008).
8. **Chih-Hung Yen,** «Investigation of AlGaInP-based Light-Emitting Diodes and GaAs-based Optoelectronic Switching Devices», Ph.D. Thesis Institute of Microelectronics, Department of Electrical Engineering, National Cheng Kung University Tainan, Taiwan (2009).
9. **Der-Feng Guo,** *ECS Transactions* 28 (4), pp. 111-118 (2010).

2.3

1. **C. M. Sun et al.,** Nuclear Instruments & Methods in Physics Research A, Vol. 547, pp. 437 - 449 (2005).
2. «Infrared HgCdTe Optical Detectors» Book Chapter, Book Title «Optoelectronic Devices Advance Simulation and Analysis», Springer New York, pp. 381-403 (2005).
3. Zhou Quan et al., Journal of Semiconductors, Vo. 34, No. 7, pp. 074010-1-4 (2013).

2.4

1. **P. Papadopoulou, L. Georgopoulos,** Journal of Engineering Science and Technology Review, Vol. 2, pp. 157-164, (2009).

2.6

1. **V. Janardhanam, Yeon-Ho Kil, Kyu-Hwan Shim, V. Rajagopal Reddy and Chel-Jong Choi**, Materials Transactions, Vol.54 No.07 (2013) pp.1067-1072 **.**

July 2015

RESEARCHE PROJECTS

1. **1/4/2014 to 30/6/2015** *Project name* : “Ship’s Health Condition, Operation Status and Performance Remote Monitoring Based on wireless sensor network and technical experience management system – MariBrain” in the frame of Synergasia 2011, Greek Ministry of Culture, Education and Religious Affairs, General Secretariat For Research & Technology.

2. **September 2008-2009,** Scientific Person in charge, *Project name*: «Silicon Bulk-Barrier Diodes designed in planar technology». Research work supported by the Research and Fund Administration Committee of Technological Education Institute of Kavala.

3. **September 2003,** Scientific Person in charge of the Department of Science of T.E.I. Kavala’s, *Project name*: «Additional educational equipment of departments in higher education».

4. **1 -7 - 1999 to 29- 6 - 2001,** *Project name*: «Improvement of infrastructure of the Laboratory of Electrical and Electronic Materials Technology, of the Department of Electrical and Computer Engineering of Democritus University of Thrace». Research work supported by the Research and Fund Administration Committee of Democritus University of Thrace.

5. **May 1, 1998 - April 30, 1999,** *Project name:* «Design, fabrication, study and optimization of silicon photo diode with high quantum efficiency to the blue spectra of visible light». Research work supported by the Greek General Secretariat of Research and Technology.*Contractor:* DEMOCRITUS University of Thrace, Department of Electrical and Computer Engineering.

6. **1 -3 - 1997 to 31- 12 - 1997,** *Project name:* «Low power design. High level power consumption of digital processing». Research work supported by the Research and Fund Administration Committee of Democritus University of Thrace.

7. **13 - 6 - 1996 to 12- 10 - 1996,** *Project name:* «Growth, modelling and simulation of SiO_2 thin films with the technique of thermal oxidation». Research work supported by the Research and Fund Administration Committee of Democritus University of Thrace.

LANGUAGES

- English

Brief Analysis of Scientific Publications

1. «Design, Fabrication, Characterization and Simulation of silicon p^+np Bulk - Barrier diodes», Ph. D. thesis, Laboratory of Electrical and Electronic Materials Technology, Department of Electrical and Computer Engineering, Democritus University of Thrace, Xanthi, Greece.

ABSTRACT: Bulk- Barrier Diodes (BBDs) are two - terminal three-layer structures similar to Bipolar Junction Transistors (BJT's) of p^+-n-p or n^+-p-n type structures. However, contrary to the BJT's, the middle (base) region in BBDs is so thin that it is normally fully depleted from free carriers, and also there exist no neutral region even for zero bias conditions (thermal equilibrium). As a result, a potential barrier is located inside the semiconductor. This potential barrier controls exponentially the current through the device. The potential barrier height can be controlled by well controllable technological parameters, such as dopant concentration and middle layer width, as well as by the applied bias voltage. This advantage and the fact that Bulk Barrier Diodes are majority carrier devices make them very attractive in many applications such as in high-speed applications or as photodiodes with high internal gain.

So far, there are several published works, dealing with some very interesting applications of BBD's, based on the initially presented theoretical models such as the model of the dc electrical behavior or the theoretical model of the optoelectronic behavior. Although most experimental results can be well explained by the above models, these models do not include the effects of all technological parameters as well as the effects of applied bias conditions. Furthermore, no analytical model has been presented, that could describe one of the most important applications of BBD, which is its application as high speed switching device (switching behavior).

The present work attempts to give solution to the above problems, using the device simulation as the basic tool. Thus, it attempts to extend and complete the

previous presented theoretical models with new analytical expressions of all the important quantities that describe the behavior of these structures, to investigate the validation limits of the new proposed models, as well as to optimize the performance of these devices in the different application areas.

More specific the present work can be divided into the following sections:

1. Extensive study, for the first time using device simulation, of the dc electrical behavior of silicon p^+-n-p type BBD, in order to complete – extend the previously presented model, as well as to investigate the validation limits of the new proposed model taking into account the fabrication parameters or / and the operation parameters (applied bias).
2. Extensive study of the switching behavior of silicon p^+-n-p type BBD, using device simulation techniques in order to introduce, for the first time, a theoretical model that could describe sufficiently the simulation and experimental results and to give solution to the optimisation of BBD in order to improve their performance (speed) for their application as switching devices.
3. Extensive study, for the first time using device simulation, of the optoeletronic behavior of silicon p^+-n-p type BBD, in order to complete – extend the previous presented model, as well as to investigate the validation limits of the new proposed model taking into account the fabrication parameters or / and the operation parameters (applied bias, illumination conditions).
4. Fabrication and characterization of a set of silicon p^+-n-p type BBD's, in order to verify the predictions of the proposed theoretical models.

Study of the dc electrical behavior of silicon p^+-n-p type BBD's

A result of this study was the introduction of a new analytical model, which extends and completes the previous model. More specifically the extensions of the new analytical model can be focused in the following point:

- Potential Barriers Φ_{BL0}, Φ_{BL} and Φ_{BR}. Introduction of analytical equations that could calculate the potential barrier heights in all bias conditions taking into account, for the first time, all the device technological parameters.
- Determination of the limits of BBD operation. The limits of BBD operation were determined, for the first time, taking into account all the device technological parameters.
- Definition of the ideality factor, η, of BBD's. The ideality factor, η, as a function of the device technological parameters was defined. The introduction of this new factor is very important in order to improve the accuracy of the new theoretical model results.
- Definition of the barrier height reduction rate with the applied voltage ($d\Phi_{BL}/dV$). Introduction of the barrier height reduction rate ($d\Phi_{BL}/dV$) as a function of the device technological parameters as well as of the applied bias conditions. In this

way we have the ability of the best explanation of the BBD's current – voltage characteristics (I-V), especially in the reverse bias conditions.

- Validation of the drift – diffusion current transport mechanism as the predominant current mechanism. The drift – diffusion current transport mechanism was verified as the predominant current transport mechanism in BBD's in the case where the middle layer width is greater than the mean free path of majority carriers (40-60 Å).

The most important conclusions of this study are the following:

1. The potential barrier heights, Φ_{BL0}, Φ_{BL} and Φ_{BR}, are mainly functions of the technological parameters N_C/N_B ratio and of middle layer width d.
2. For given values of N_E and N_C, the limits of BBD operation can be controlled by the values of d and N_B.
3. The barrier height reduction rate ($d\Phi/dV$), with respect to the applied bias voltage, depends strongly on the ratio N_C/N_B and on the applied bias conditions.
4. The presence of free carriers in the space-charge regions strongly affects the mean total charge densities in these regions and, consequently, the barrier height, the N_C/N_B ratio, the barrier height reduction rate ($d\Phi/dV$) and ideality factor, η, of BBDs.

Study of the switching behavior of silicon p^+-n-p type BBD's.

A result of this study was the introduction, for the first time, of a theoretical model, which describes sufficiently the switching behaviour of silicon p^+-n-p type BBD. This new model calculates sufficiently the switching time, τ_{SW}, of BBD's taking into account the technological parameters, as well as the operational parameters such as bias conditions.

The most important conclusions of this study are the following:

1. BBDs, as majority carrier devices, exhibit no minority carrier storage effect in the limit of the depletion region and, therefore, can operate with inherently fast response (τ_{STOR} extremely small).
2. The trapping time, τ_{TRAP}, of free electrons in the potential well remains extremely small even for very large values of the applied bias voltage, due to their low concentration compared with the middle layer donor's concentration.
3. The transit time of the depletion region, τ_{TRANS}, which is the time required by the carriers to traverse the depletion region, remains also extremely small ($\tau_{TRANS} <$ 10ps), due to high internal fields and small depletion region widths.
4. The BBDs switching time, τ_{SW}, is mainly determined by the charging-discharging time constant ($\tau \sim RC$) of the depletion layer capacitance, C_j, through the total finite resistance R, which is the parallel combination of the device series resistance R_S and of the dynamic (differential) resistance R_D.
5. The BBD switching time is a function of the technological parameters N_B, N_C, and d and, thus, by the appropriate choice of these parameters the BBD switching time can be reduced in the picosecond range.

6. The BBD switching time, τ_{SW}, may also be reduced by the increasing reverse bias voltage due to the decrease of the depletion layer capacitance, C_j.

Study of the optoelectronic behavior of silicon p^+-n-p type BBD's

A result of this study was the introduction of a new analytical model, which extends and completes the previously published model. More specifically the extensions of the new analytical model can be focused in the following point:

- Calculation of the barrier lowering, $\Delta\Phi_{BL}$, under illumination conditions. Extension of previously published theoretical model of the barrier lowering, $\Delta\Phi_{BL}$, with the introduction of the new factor, m, which found to be a function of the applied bias voltage as well as of the incident light optical power density P_i. Also, validation of the theoretical model the limits, concerning the values $\Delta\Phi_{BL}$, I_{PH} and η_{ext}, were determined, for the first time, taking into account the incidence optical power level. The introduction of this new factor as well as the determination of validation of the theoretical model limits, sufficiently contribute in the explanation of the experimental results which were difficult to explain with the previously published theoretical model.
- Optimization of the external quantum efficiency. The dependency of the external quantum efficiency by, the technological parameters, the incident light wavelength, the optical power density and light modulation frequency as well as the bias conditions was investigated. The determination of the dependency of the external quantum efficiency by all these parameters offers the ability to fabricate BBD photodiodes with desirable properties.

The most important conclusions of this study are the following:

1. The silicon p^+-n-p type Bulk-Barrier photodiodes are majority carrier photodetectors with high internal gain.
2. Bulk-Barrier photodiodes exhibit very high and uniform external quantum efficiency in the blue, green and red region of the visible spectrum, compared to the common silicon photodiodes. The uniform and high quantum efficiency of BBD photodiodes makes them very attractive devices for optical video applications.
3. The external quantum efficiency of the Bulk-Barrier photodiodes increases as the incident optical power level decreases. This makes BBDs very useful devices for low optical power applications.
4. The reduction of the middle layer width, *d*, leads to an increase of the Bulk – Barrier photodiodes speed, for given operational conditions (bias conditions, incident light wavelength and optical power density).
5. The external quantum efficiency of BBD's significantly affected by the middle layer width, *d*, and doping concentration, N_B, as well as by the emitters doping concentration, N_E. An increase of all these parameters leads to an increase of the external quantum efficiency.

Fabrication and characterization of silicon p+-n-p type BBDs

BBDs were fabricated with the ion implantation technique using Rapid Thermal Annealing, (RTA), process for the fabricated device annealing. The fabricated BBDs were characterized electrically and optoelectronically and their speed was also measured using electrical and optical pulses. The experimental results show that the technological and operational parameters significantly affect the electrical, switching and optoelectronic behavior of BBDs agreeing well with the predictions of the theoretical models proposed in the present work.

REACHERS PAPERS

2.1. **P. Papadopoulou, N. Georgoulas, L. Georgopoulos, A. Thanailakis, 2001, "A model for the dc electrical behaviour of Bulk-Barrier Diodes",** Electrical Engineering, Archiv für Elektrotechnik, Vol. 83 (4), pp. 203-211 (2001).

Abstract: This paper presents a complete analytical model for the dc electrical behavior of Bulk Barrier Diodes (BBD's). The proposed model extends the previous presented models and gives analytical expressions for all significant magnitudes for dc device performance, as barrier height, current density and ideality factor, with respect to the technological parameters and the applied voltage in both bias conditions. The theoretical results have been compared to those obtained by the 2-D physical based device simulator S-PISCES, which takes into account drift - diffusion theory, concentration and field depended mobility, Shockley–Read–Hall and Auger recombination and band gab narrowing models. Good agreement was obtained between theory and simulation. Through the simulator the effect of the free carriers on the dc behavior of BBD's with respect to technological parameters and applied voltage is understood in greater details.

2.2. **P. Papadopoulou, N. Georgoulas and A. Thanailakis, "Simulation and Experimental Results on the Switching Behaviour of Bulk-Barrier Diodes".** Microelectronics Journal, Vol. 33 (5-6), pp. 487-494 (2002).

Abstract: In this paper, the switching behavior of Bulk Barrier Diodes (BBD's), as a function of technological parameters has been studied. This study was based on the transient simulation analysis of BBD's structures using the 2-D device simulator S-PISCES. The simulation shows that the technological parameters and bias conditions

have a significant effect on the switching behavior of BBD's. The result of this study is the proposal of an analytical model that describes satisfactorily the BBD's switching behavior. Good agreement was obtained between simulation and analytical results and as this study shows, by suitable selection of technological parameters the switching time of BBD's can be reduced in the picosecond range.

2.3. **P. Papadopoulou, N. Georgoulas and A. Thanailakis, " An extensive study of the photocurrent amplification mechanism of silicon Bulk - Barrier diodes based on simulation and experimental results",** Thin Solid Film, Vol. 415, pp. 276-284 (2002).

Abstract: In this paper, an extensive study of the photocurrent amplification mechanism of silicon Bulk – Barrier Diodes (BBDs) is presented, based on simulation and experimental results. As a result of this study an analytical model is proposed. The proposed model extends previously published models and includes analytical expressions for all significant quantities of the device optoelectronic behaviour. Such quantities are barrier lowering, photocurrent, quantum efficiency and response speed as functions of the applied voltage, incident light power, light wavelength and modulation frequency, as well as a function of technological parameters. Simulation and experimental results verify the validity of the proposed analytical model, and they show that BBDs are majority carrier photodetectors with high internal photocurrent gain. Compared with common photodetectors, BBDs exhibit a very high sensitivity in the blue region of the visible spectrum.

2.4. **P. Papadopoulou, N. Georgoulas , L. Magafas, «A study of the optical response speed of silicon Bulk -Barrier photodiodes based on simulation results»,** OPTOELECTRONICS AND ADVANCED MATERIALS - RAPID COMMUNICATIONS Vol. 1, No. 8, p. 379 -384 (2007).

Abstract: In this paper, an extensive study of the transient optical response speed of silicon Bulk–Barrier Diodes (BBDs) is presented. This study is based on the simulation results obtained with a 2-D device simulator (S PISCES and LUMINOUS). The influence of significant quantities, as the applied voltage, the incident light power and the light wavelength, on the optical response speed of silicon Bulk–Barrier Diodes was investigated. As a result of this study we propose a model that calculates the cut–off frequency (optical response speed) of silicon BBDs when a

modulated light is applied. Simulation results verify the validity of the proposed model and show that it is possible to achieve high speed optical response by choosing appropriate operational parameters.

2.5. **P. Papadopoulou, Ant. Meletis, G. Doukakis, C. Mertzanidis, «Frequency Domain Response of Dielectrics for TE Plane Waves»,** European Journal of Scientific Research, Vol. 34, No.4, pp. 463-473 (2009).

Abstract: Some special characteristics of electromagnetic response of stratified dielectric structures in the frequency domain are studied. We consider Transverse Electric type plane waves incident obliquely on dielectric slabs or more complicated half spaces. The study of zeros and periodicities in these configurations can show the similarities as well as the differences from the Transverse Magnetic type plane waves. The role of non – ideal dielectrics is catalytic, because it causes the degeneration of both the zeros and the periodicities of the reflection coefficient.

2.6. **P. Papadopoulou, L. Georgopoulos «A study of the silicon Bulk-Barrier Diodes designed in planar technology by means of simulation»** Journal of Engineering Science and Technology Review, Vol. 2, pp. 157-164, (2009).

Abstract: In this paper, it is studied for the first time, the possibility of manufacturing a Bulk Barrier diode in planar technology using simulation. This study is based on simulation results obtained with a 2-D device simulator (S-PISCES). More precisely, the electrical and switching behavior of the proposed devices in planar technology were investigated. The results of this study show that the technological parameters (doping concentrations), as well as the geometrical sizes (middle region width) and the bias conditions (applied voltage), have significant effects on the electrical and switching behavior of the proposed devices. The appropriate choice of these parameters can reduce the switching time in the range of few picoseconds and also dramatically modify the current through the device. The simulation results of devices in planar technology have been compared with those designed in non planar technology. Finally, good agreement among theory and simulations results of the proposed devices observed.

2.7. **M.Hanias, L.Magafas, S.Stavrinides, P.Papadopoulou and M.Ozer, «Chaotic behavior of the forward I-V characteristic of the Al/a-SiC:H/c-Si(n) heterojunction Complexity»,** Proceedings of the 4th International Interdisciplinary Chaos Symposium, p.221,(2013).

Abstract: In this paper the electrical behavior of the Al/a-SiC:H/c-Si(n) heterojunction for different values of density of gap states (N) in a-SiC:H, is simulated and studied. It is observed that as the density of gap states in a-SiC:H increases from 10^{-15} cm^{-3} to 10^{-18} cm^{-3} the I-V characteristics, in the forward bias, present a deviation from the typical I-V of a diode, which is enhanced with the increase of N. For $N_D = 10^{-18}$ cm^{-3} the forward I-V characteristic shows strong chaotic vibration that is attributed to the tunneling effect taking place in the junction a-SiC:H/c-Si(n) in the forward bias. With the method of delays correlation and minimum embedding dimension are calculated, while the influence of gap states in strengthening chaos is studied.

2.8. **P. Papadopoulou, S. Stavrinides, M. Hanias, L. Magafas, «Study of the Electrical Behavior of Metal/_-SiC:H/poly-Si(N) Structure Using Simulation»,** Proceedings of the 4th International Congress APMAS2014, Acta Physica Polonica, Vol. 127 no 4 (2015).

Abstract: In this report, a study of the electrical behavior for the Metal/a-SiC/poly-Si(n) structure, appears. Different thicknesses of a-SiC:H thin films are considered; in specific the a-SiC:H layer thickness is varied between 100 Å up to 800 Å. The 2-D ATLAS advanced numerical simulator has been utilized in order to simulate the material's electrical behaviour and produce the reported hereby results. The study of the I-V (current-voltage) characteristics of these Metal/a-SiC:H/poly-Si(N) structures, reveals a very interesting hysteretic behaviour that is a function of the a-SiC:H thin-flm thickness. Such materials have lately raised the engineering community's interest because of their possible utilization as memristive elements.